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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,095	06/11/2002	Chih-Wei Hung .	9068-US-PA	7113

31561 7590 11/15/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
MUNSON, GENE M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/15/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/064,095
Filing Date: June 11, 2002
Appellant(s): CHIH-WEI HUNG

Belinda Lee
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 9, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal. Accordingly, there is no Related Proceedings Appendix.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The Brief is deficient because the Brief (page 2) does not explain that the "local interconnect ... extending to an upper portion of the isolation structure to cover a periphery of the isolation structure" limitation of independent claim 1 is shown by conductive layer 212 over the periphery of the isolation structure 204, between photodiode 206 and gate of source follower transistor 222, in Figure 2 (see page 7, ¶ 24, lines 14-16). The conductive layer 212 caps a periphery of the isolation structure 204, between photodiode 206 and gate of source follower transistor 222.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims 1-7 and 16 contained in the Appendix to the Brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

6,392,263	Chen et al	5-2002
6,649,950	He et al	11-2003 (parent filed 11-2001)
6,740,915	Rhodes	5-2004 (filed 11-1998)

(9) Ground of Rejection

Claims 1-7 and 16 are rejected under 35 USC 103 as unpatentable the evidence being He et al, Chen et al '263 and Rhodes '915, all considered together. For an image device pixel as in Chen et al (Figure 1C), with the photodiode and reset transistor as in He et al (Figure 2), it would have been obvious to use an "interconnect" 320 as in Rhodes, "extending to an upper portion of the isolation structure" 132, 332 as in Rhodes, in order to connect the n-type "source" region 201 of the "reset" transistor as in He et al to the gate of a "source follower" transistor as in Rhodes and Chen et al. The "photodiode sensing" region reads on a photodiode region 103 as in He et al. The n-type region 201 as in He et al (Figure 2) corresponds to a region 30 as in Rhodes (Figure 1) and region 315 as in Rhodes (Figure 11), and to the node between photodiode 103 and reset transistor 101a as in Chen et al (Figure 1C). The conductor layer 320 as in Rhodes (Figure 11) corresponds to the connection 44 between region 30 and "source follower" transistor 36 as in Rhodes (Figure 1), and to the connection between photodiode 103 and "source follower" transistor 104 as in Chen et al (Figure 1C).

The "isolation structure" reads on a field oxide FOX as in He et al and field oxide 132, 332 as in Rhodes, which would have been obvious to use for isolation. A field oxide FOX as in He et al is "over the photosensing region" 103, as claimed. The claimed "periphery of the isolation structure" reads on a field oxide 132, 332 (Figure 5, column7, lines 8-20; Figure 11, column 10, lines 13-31) as in Rhodes, which would have been obvious to use for isolation between a photodiode 103 and the gate of a source follower transistor 104, as in Chen et al (Figure 1C). Thus, He et al and Rhodes together would have suggested a field oxide "isolation structure over the photosensing region," as in He et al (Figure 2), where also a field oxide "periphery of the isolation structure" is used between a "photodiode sensing" region and the gate of a "source follower" transistor, as in Rhodes (Figure 11). As claimed, Rhodes (Figure 11)

shows a "first end of the local interconnect" 320 at 315, a "periphery of the isolation structure" at 332, and a "second end of the local interconnect" 320" at "source follower" transistor area 330.

Note that in Rhodes, region 315 in Figure 11 corresponds to region 30 in Figure 1, which is a source region of reset transistor 31. Reset transistor 104 of present invention (Figure 1) corresponds to reset transistor 31 of Rhodes (Figure 1), reset transistor 101a of Chen et al (Figure 1C), and the reset transistor of He et al (Figure 2). Photodiode 102, 206, 306 of present invention (Figures 1, 2, 3F) corresponds to photodiode 103 of Chen et al (Figure 1C), photodiode 350, 352 of Rhodes (Figure 11), and photodiode 103 of He et al (Figure 2). Source follower transistor 106 of present invention (Figure 1) corresponds to source follower transistor 36 of Rhodes (Figure 1) and source follower transistor 104 of Chen et al (Figure 1C). Conductive layer 212 of present invention (Figure 2) corresponds to conductive layer 320 of Rhodes (Figure 11).

The conclusion is that the claimed invention as a whole would have been obvious at the time the invention was made. The hypothetical person of ordinary skill in the art, familiar with all that He et al, Chen et al '263 and Rhodes '915 disclose, "would have found it obvious to make a structure corresponding to *what is claimed*." *In re Sovish*, 226 USPQ 771, 774 (Fed. Cir. 1985).

(10) Response to Argument

The Brief (page 6) agrees that the "local interconnect" layer 212 (Figures 2, 3F) does not extend to cover the portion of the "isolation structure over the photosensing region" 206, 306. Contrary to the Brief (page 6), the combined teachings of the references would have suggested an "isolation structure over the photosensing region," as in He et al (Figure 2), along with a "periphery of the isolation structure" to be used, as in Rhodes, for isolation between a "photodiode sensing" region and the gate of a source follower transistor, as in Rhodes and Chen et al. Contrary to the Brief (pages 6-7), the claimed "local interconnect" reads on a conductive

layer 320 as in Rhodes (Figure 11), which simply implements an interconnection between a photodiode and the gate of a source follower transistor, as taught in Rhodes and Chen et al.

Contrary to the Brief (pages 6-7), one cannot show non-obviousness by attacking He et al, Chen et al and Rhodes individually where, as here, the rejection is based on the combined teachings of the references. *In re Keller*, 208 USPQ 871, 881, 882 (CCPA 1981).

It is submitted that the claims on appeal are properly rejected as unpatentable, as explained above.

Respectfully submitted,

Gene M. Munson

GENE M. MUNSON
EXAMINER
GROUP ART UNIT 2811

Conferees:

Richard Elms

Darren Schuberg